

The listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

1. (Previously Presented) A resistive memory device comprising:

a conductive bottom electrode having a top surface;

a multi-resistive state element having a top surface and a bottom surface, the bottom surface of the multi-resistive state element arranged on top of and in direct physical contact with the top surface of the conductive bottom electrode, the multi-resistive state element having a substantially crystalline layer that, while substantially maintaining its substantially crystalline structure, has a modifiable resistance;

a conductive top electrode having a bottom surface and arranged on top of and in direct physical contact with the top surface of the multi-resistive state element, wherein the resistance of the resistive memory device may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes;

a top interface created by the direct physical contact between the bottom surface of the top electrode and the top surface of the multi-resistive state element; and

a bottom interface created by the direct physical contact between the top surface of the bottom electrode and the bottom surface of the multi-resistive state element, at least one of the top interface or the bottom interface includes at least one treatment primarily directed towards changing properties of the at least one interface, and

whereby the properties of the at least one interface are changed by the at least one treatment.

2. (Original) The resistive memory device of claim 1, wherein:  
the at least one treatment is an ion implant.
3. (Previously Presented) The resistive memory device of claim 1, wherein:  
the at least one treatment is an exposure to an anneal.
4. (Previously Presented) The resistive memory device of claim 3, wherein:  
the anneal is performed while the multi-resistive state element is formed.
5. (Previously Presented) The resistive memory device of claim 1, wherein:  
the at least one treatment is an exposure to a gas.
6. - 7. (Cancelled)
8. (Previously Presented) The resistive memory device of claim 3, wherein:  
the anneal is performed after the conductive bottom electrode is formed.
9. (Previously Presented) The resistive memory device of claim 3, wherein:  
the anneal is performed after the multi-resistive state element is formed.
10. (Previously Presented) The resistive memory device of claim 3, wherein:  
the anneal is performed after the conductive top electrode is formed.
11. (Previously Presented) The resistive memory device of claim 5, wherein:  
the exposure to the gas causes a chemical reaction in the multi-resistive state material.

12. (Previously Presented) The resistive memory device of claim 5, wherein:  
the exposure to the gas is performed after the conductive bottom electrode is formed.

13. (Previously Presented) The resistive memory device of claim 5, wherein:  
the exposure to the gas is performed after the multi-resistive state element is formed.

14. (Previously Presented) The resistive memory device of claim 5, wherein:  
the exposure to the gas is performed after the conductive top electrode is formed.

15. - 18. (Cancelled)

19. (Previously Presented) The resistive memory device of claim 1, wherein:  
the at least one treatment is caused by a chemical reaction between one of the conductive electrodes and the multi-resistive state element.

20. (Original) The resistive memory device of claim 19, wherein:  
an anneal process is a catalyst for the chemical reaction.

21. (Original) The resistive memory device of claim 19, wherein:  
an exposure to a gas is a catalyst for the chemical reaction.

22. (Original) The resistive memory device of claim 1, wherein:  
the at least one treatment is caused by a plasma process.

23. (Original) The resistive memory device of claim 22, wherein:  
the plasma process is a plasma etch.
24. (Previously Presented) The resistive memory device of claim 1, wherein:  
both the bottom interface and the top interface are subject to a treatment, the  
treatments being different from each other.
25. (Original) The resistive memory device of claim 1, wherein:  
the at least one treatment is caused by re-sputtering.
26. (Previously Presented) The resistive memory device of claim 1, wherein:  
the at least one treatment is caused by a bombardment by inert ions.
27. (Previously Presented) The resistive memory device of claim 1, wherein:  
the at least one treatment is caused by a laser treatment.

28. (Previously Presented) A resistive memory device comprising:

a conductive bottom electrode having a top surface;

a multi-resistive state element having a top surface and a bottom surface, the bottom surface of the multi-resistive state element arranged on top of and in direct physical contact with the top surface of the conductive bottom electrode, the multi-resistive state element having at least one layer that is fabricated to be substantially crystalline and have a programmable resistance;

a conductive top electrode having a bottom surface and arranged on top of and in direct physical contact with the top surface of the multi-resistive state element, wherein the resistance of the resistive memory device may be programmed by applying a first voltage having a first polarity across the conductive electrodes and reversibly programmed by applying a second voltage having a second polarity across the conductive electrodes;

a top interface created by the direct physical contact between the bottom surface of the conductive top electrode and the top surface of the multi-resistive state element; and

a bottom interface created by the direct physical contact between the top surface of the conductive bottom electrode and the bottom surface of the multi-resistive state element, at least one of the top interface or the bottom interface includes a treatment primarily directed towards changing properties of the at least one interface, and

whereby the properties of the at least one interface are changed by the treatment.

29. (Previously Presented) The resistive memory device of claim 28, wherein:  
the at least one layer that is fabricated to be substantially crystalline is fabricated to be polycrystalline.
30. (Previously Presented) The resistive memory device of claim 28, wherein:  
the at least one layer that is fabricated to be substantially crystalline is fabricated to be a perovskite.
31. (Previously Presented) The resistive memory device of claim 30, wherein:  
the at least one interface that is subjected to the treatment is directed towards changing properties of the perovskite.